IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A semiconductor memory device comprising:

a semiconductor substrate;

a first insulation layer formed on an inner surface of a trench formed in the semiconductor substrate and having its top located above the surface of the semiconductor substrate;

a diffusion layer formed within the semiconductor substrate, surrounding the deep portion of the trench;

a first conductive layer filled in the trench;

a gate electrode provided on a gate insulation layer formed on the surface of the semiconductor substrate;

source/drain diffusion layers formed in the surface of the semiconductor substrate, sandwiching a channel region below the gate electrode; and

a second conductive layer extending on the first conductive layer, the first insulation layer, and one of the source/drain diffusion layers.

Claim 2 (Original): The device according to claim 1, wherein the first insulation layer is provided on the inner surface of the trench without exposing a side of the semiconductor substrate within the trench.

Claim 3 (Original): The device according to claim 2, wherein the second conductive layer is provided without contacting the side of the semiconductor substrate.

Claim 4 (Original): The device according to claim 1, wherein a top of the first conductive layer is located above the surface of the semiconductor substrate.

Claim 5 (Original): The device according to claim 1, further comprising a second insulation layer overlying the top of the first insulation layer.

Claim 6 (Original): The device according to claim 1, further comprising a third insulation layer provided on the first conductive layer and consisting of a same material of the first insulation layer.

Claim 7 (Original): The device according to claim 6, further comprising a device isolation insulation layer consisting of a same material as the first and third insulation layers and having in its surface a concave whose bottom is located above the surface of the semiconductor substrate.

Claim 8-18 (Canceled)

Claim 19 (New): The device according to claim 1, wherein an end of the one of the source/drain diffusion layers on which the second conductive layer extends contacts a side of the first insulation layer.

Claim 20 (New): The device according to claim 1, wherein the second conductive layer electrically connects the first conductive layer to the one of the source/drain diffusion layers on which the second conductive layer extends.

Claim 21 (New): A semiconductor memory device comprising:

a semiconductor substrate;

a first insulation layer formed on an inner surface of a trench formed in the semiconductor substrate and having its top located above a surface of the semiconductor substrate;

a diffusion layer formed within the semiconductor substrate, surrounding the deep portion of the trench;

a first conductive layer filled in the trench;

a gate electrode provided on a gate insulation layer formed on the surface of the semiconductor substrate, a bottom surface of the gate electrode being lower than a top surface of the first conductive layer;

source/drain diffusion layers formed in the surface of the semiconductor substrate, sandwiching a channel region below the gate electrode; and

a second conductive layer extending on the first conductive layer, the first insulation layer, and one of the source/drain diffusion layers.

Claim 22 (New): The device according to claim 21, wherein the first insulation layer is provided on the inner surface of the trench without exposing a side of the semiconductor substrate within the trench.

Claim 23 (New): The device according to claim 22, wherein the second conductive layer is provided without contacting the side of the semiconductor substrate.

Claim 24 (New): The device according to claim 21, wherein a top of the first conductive layer is located above the surface of the semiconductor substrate.

Claim 25 (New): The device according to claim 21, further comprising a second insulation layer overlying the top of the first insulation layer.

Claim 26 (New): The device according to claim 21, further comprising a third insulation layer provided on the first conductive layer and consisting of a same material of the first insulation layer.

Claim 27 (New): The device according to claim 26, further comprising a device isolation insulation layer consisting of a same material as the first and third insulation layers and having in its surface a concave whose bottom is located above the surface of the semiconductor substrate.

Claim 28 (New): The device according to claim 21, wherein an end of the one of the source/drain diffusion layers on which the second conductive layer extends contacts a side of the first insulation layer.

Claim 29 (New): The device according to claim 21, wherein the second conductive layer electrically connects the first conductive layer to the one of the source/drain diffusion layers on which the second conductive layer extends.